Demo Carrier Board for Industrial Micromodule

Overview

The Trenz Electronic TE0304 Demo Carrier Board provides low-cost connection and extension to the Trenz Electronic TE0300 Spartan-3E Industrial Micromodule series.

The TE0300 micromodule signals are available on high-density, surface mount connectors and are routed to the standard headers of the Demo Carrier Board with a differential impedance of 100 ohm.

The following ports are available for application demonstration: one D-sub 15-pin VGA output, two D-sub 9-pin RS-232 ports, two PS/2 ports.

A 14-pin JTAG connector for Xilinx parallel cable III, IV and USB cable HW-USB is made available for easy attachment

Flexible power supply is possible through screw terminals (J7), dedicated DC jack (J8) or optionally USB bus (J12).

Features

- FPGA signals available on header J2 and J4, each with 2 x 20 pin 2.54 mm (100 mil) pitch
- 23 differential pairs (for high-speed signals)
- 10 single-ended lines (for low- / medium-speed signals)
- 1 x 12-pin Pmod or, alternatively, up to 2 x 6-pin Pmods
- header connector J5 with 2 x 20-pin 1.27 mm (50 mil) pitch for the direct connection with an Optomotive Cameleon camera head
- Board power supply via screw terminals, DC jack or optionally industrial USB connector
- JTAG header compatible with Xilinx parallel cable III, IV and USB cable HW-USB
- Small form factor: 115 x 79 mm

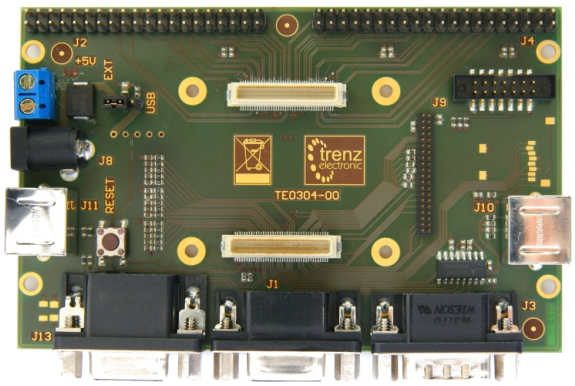


Figure 1: demo carrier board: top view without TE0304 module.

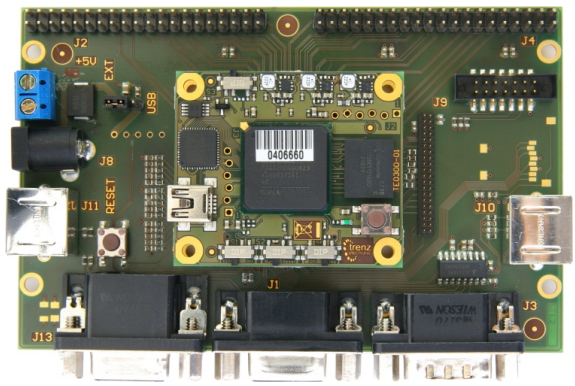


Figure 2: demo carrier board: top view with TE0304 module.

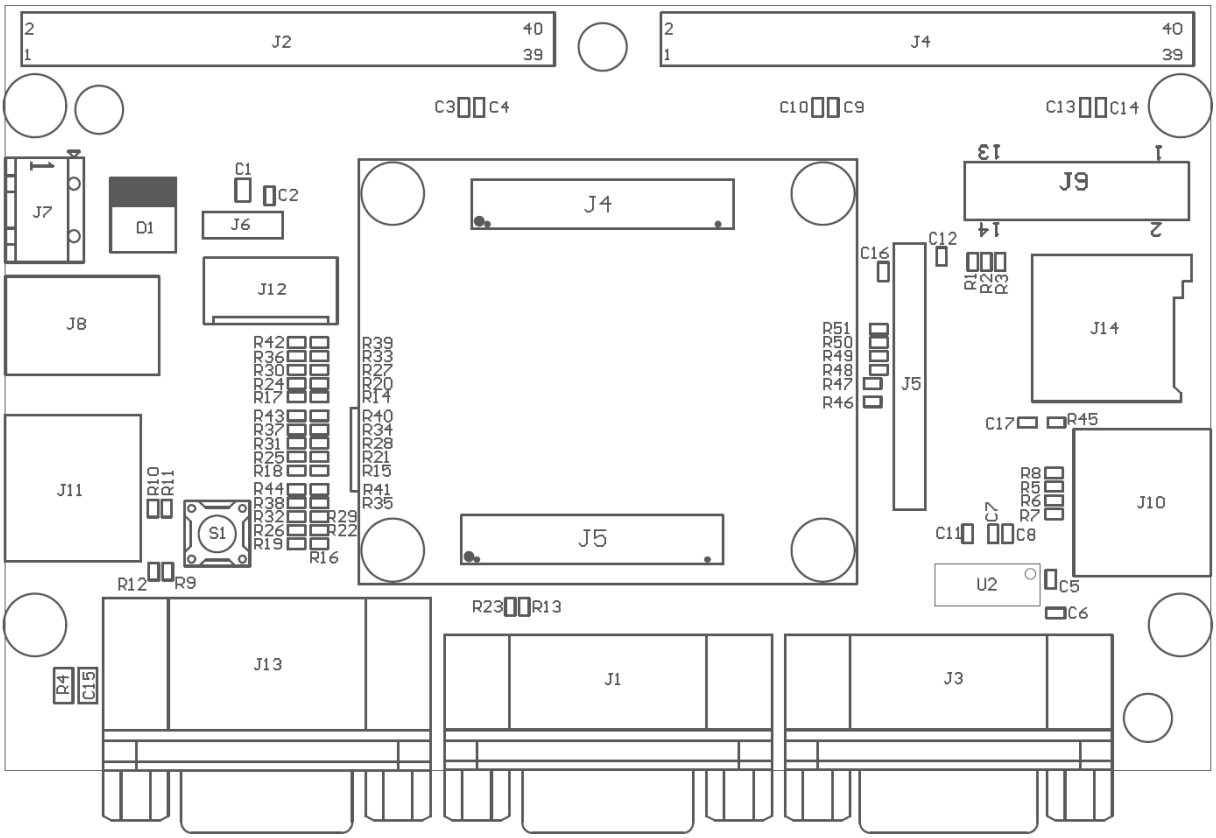


Figure 3: assembly diagram.

Details

To locate jumper and connectors, see Figure 3: assembly diagram.

Warning: make sure to install the module only in the way shown in Figure 2!

A quick way to check this is to make sure that the mounting holes on the TE0300 micro-module are in line with those on the TE0304 Demo Carrier Board.

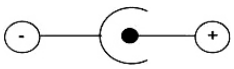
Power Supply

There are three ways to supply power to the board:

- 5 V DC power supply
- USB bus power supply (optional).

5 V DC power supply

Set the Jumper J6 [TE0304] to EXT, and connect a 5 V DC supply to either the 2.5 mm DC-jack J8 [TE0304] (center positive) or the DC screw terminals J7 [TE0304] (upper positive as hinted by the "+5V").



Both inputs are protected against polarity inversion by a cross bar diode D1. Screw terminals J7 [TE0304] are not populated by default.

USB bus power supply (optional)

Set the Jumper J6 [TE0304] to USB and connect a USB host-powered cable to the industrial USB receptacle J12 [TE0304]. Receptacle J12 [TE0304] is not populated by default. For further information, please consult paragraph "USB Port".

Header Power Pins

Power pins on the I/O mating headers can provide power to external circuits. The following voltages are generated on the micromodule:

- 1.2 V (J4 [TE0304]: 33, 34)
- 2.5 V (J4 [TE0304]: 13, 14)
- 3.3 V (J2 [TE0304]: 3, 4, 33, 34).

For more information on available power ratings, please see "Trenz Electronic TE0300 Industrial Micromodule User Manual".

I/O Banks Power Supply

Power supply input VccIO for FPGA bank 0 can be connected externally through connector J2, pins 1-2 (VccIO0). If bank 0 is not needed, VccIO can be left open.

Warning! If the VccIO line is supplied internally by one of the power-supply lines present on the TE0300 module, do NOT apply any external voltage.

Warning! Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see Xilinx Answer AR#19146).

Single-ended lines

The demo carrier board has a total of 10 single ended lines routed to header connectors J2 [TE0304] and J4 [TE0304]. These lines can be used for low-speed and medium-speed signals.

Differential Pairs

The demo carrier board has a total of 23 differential signal pairs routed with a differential impedance of 100 ohm to header connectors J2 [TE0304] and J4 [TE0304]. These lines can be used for high speed signaling up to 666 Mbit/s per differential pair (see Xilinx application note XAPP485 "1:7 Deserialization in Spartan-3E/3A FPGAs at Speeds Up to 666 Mbps", xapp485.pdf).

Application Ports

The TE0304 Demo Carrier Board provides the following ports ready for FPGA-driven applications or demonstrations:

- 1 x microSD (socket)
- 1 x Optomotive camera (male)
- 1 x 12-pin Pmod or, alternatively, up to 2 x 6-pin Pmods
- 2 x PS/2 (female)
- 1 x RS-232 DCE (female)
- 1 x RS-232 DTE (male)
- 1 x VGA (female)

Each application port is composed of a hardware interface and the corresponding FPGA core.

microSD

The FPGA can read and write at bank 2 a microSD card through the microSD socket J14 [TE304] as detailed in Table 1. The microSD socket is provided with a card detection switch (c.d.s.).

Signal	FPGA pin	FPGA ball
DAT2	IO_L20N_2	R12
CD/DAT3	IO_L18P_2	P11
CMD	IO_L18N_2	N11
VDD	3.3 V	-
CLK	GCLK15	V9
VSS	GND	-
DAT0	IO_L10P_2	R8
DAT1	IO_L10N_2	T8
c.d.s.	IP_L23P_2	V14

Table 1: microSD signal details (bank 2).

Optomotive camera

An Optomotive Cameleon camera head

can be connected to the TE0304 Demo Carrier Board through a 40-wire ribbon cable inserted on header connector J5 [TE0304] with 1.27 mm (50 mil) pitch as shown in Figure 4.

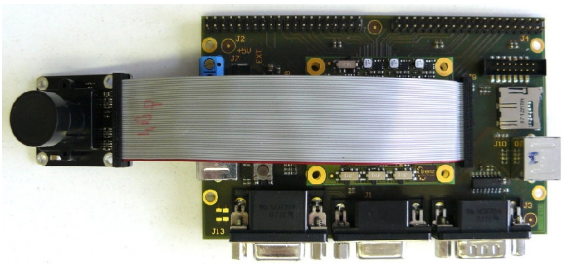


Figure 4: Optomotive camera connected to the demo board.

Please make sure that the ribbon cable connector is inserted on header connector J5 [TE0304] such that wire 1 (usually the only color-marked wire) is near the bottom part of the board (VGA and RS-232 ports side).

For further information about Optomotive technology, please read Trenz Electronic application note "TE0300 XPS Reference Designs" (AN-TE0300-01.pdf)

Pmod (peripheral module) port(s)

One 12-pin Pmod device or, alternatively, up to two 6-pin Pmod devices can be connected to a section of header connector J2[TE0304] as shown in Figure 5.

Pmod pin-out at connector J2 [TE0304]) is detailed in Table 2.

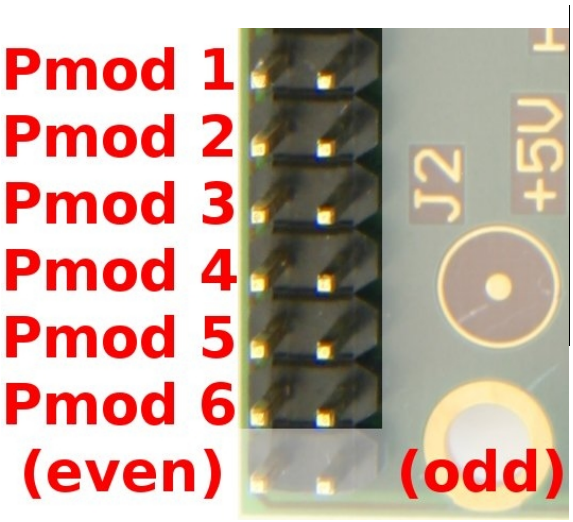


Figure 5: Pmod port(s).
Table 2: Pmod pin-out (J2 [TE0304]).

Pmod signals are available at bank 0 of the FPGA as detailed in Table 3.

Signal	FPGA pin	FPGA ball
Pmod 1 odd	IO_L20P_0	B6
Pmod 2 odd	IO_L23N_0	D5
Pmod 3 odd	IO_L24N_0	B4
Pmod 4 odd	IO_L25P_0	C3
Pmod 5 odd	GND	-
Pmod 6 odd	3.3 V	-
Pmod 1 even	IO_L20N_0	A6
Pmod 2 even	IO_L23P_0	C5
Pmod 3 even	IO_L24P_0	A4
Pmod 4 even	IO	C4
Pmod 5 even	GND	-
Pmod 6 even	3.3 V	-

Table 3: Pmod pin-out (bank 0).

PS/2 Ports

The TE0304 Demo Carrier Board is equipped with two mini-DIN-6 female connectors (J10 and J11) for the connection of serial input devices with PS/2 connectors (typically keyboard and

mouse). PS/2 signals are available at bank 2 of the FPGA as detailed in Table 4.

Signal	FPGA pin	FPGA ball
PS2_C1 (port 1 clock)	IO_L12N_2	M9
PS2_D1 (port 1 data)	IO_L07P_2	N7
PS2_C2 (port 2 clock)	IO_L04P_2	R5
PS2_D2 (port 2 data)	IO_L04N_2	T5

Table 4: PS/2 pin-out (bank 2).

RS-232 DCE Port

The TE0304 Demo Carrier Board is equipped with an RS-232 DCE (data communication equipment) serial port implemented with a D-sub 9-pin female connector J1 [TE0304] as detailed in Table 5.

Pin	Dir.	Signal
1, 4, 6	-	internally connected
2	O	TxD-DCE
3	I	RxD-DCE
5	-	GND
7, 8	-	internally connected
9	-	not connected

Table 5: pin-out of connector J1 [TE0304].

The RS-232 DCE signals are available at bank 2 of the FPGA as detailed inTable 6.

Signal	FPGA pin	FPGA ball
TxD-DCE	IO_L05N_2	P6
RxD-DCE	IO_L05P_2	R6

Table 6: RS-232 DCE signal details (bank 2).

RS-232 DTE Port

The TE0304 Demo Carrier Board is equipped with an RS-232 DTE (data terminal equipment) serial port implemented with a D-sub 9-pin male connector J3 [TE0304].

Pin	Dir.	Signal
1, 4, 6	-	internally connected
2	I	RxD-DTE
3	O	TxD-DTE
5	-	GND
7, 8	-	internally connected
9	-	not connected

Table 7: pin-out of connector J3 [TE0304].

The RS-232 DTE signals are available at bank 2 of the FPGA as detailed in Table 8.

Signal	FPGA pin	FPGA ball
TxD-DTE	IO (bank 2)	V7
RxD-DTE	IO_L07N_2	P7

Table 8: RS-232 DTE signal details (bank 2).

VGA Port

The FPGA can drive a VGA output port through a D-sub 15-pin male connector. Each RGB channel has a resolution of 5 bits, for an overall color depth of 32,768 colors per pixel.

The VGA signals are available at bank 2 and 3 of the FPGA as detailed in Table 9.

Signal	FPGA pin	FPGA ball
R0	IO_L23P_3	R3
R1	IO_L23N_3	R2
R2	IO_L21P_3	P2
R3	IO_L21N_3	P1
R4	IO_L24P_3	T2
G0	IO_L06N_2	V6

Signal	FPGA pin	FPGA ball
G1	IO_L06P_2	V5
G2	IO (bank 2)	U5
G3	IO_L03P_2	U4
G4	IO_L18N_3	M3
B0	IO_L19N_3	M6
B1	IO_L19P_3	M5
B2	IO_L17P_3	L6
B3	IO_L17N_3	L5
B4	IO (bank 2)	U6
/HSYNC	IO_L20P_3	N4
/VSYNC	IO_L20N_3	N5
VGA_SCL	IO_L22P_3	P3
VGA_SDA	IO_L22N_3	P4

Table 9: VGA port pin-out (bank 2 and 3).

Other Ports

JTAG Port

Connector J9 is a 14-pin JTAG connector for Xilinx parallel cable III, IV and USB cable HW-USB.

Pin	Signal
1	GND
2	Vref (3.3 V)
3	GND
4	TMS
5	GND
6	TCK
7	GND
8	TDO
9	GND
10	TDI
11	GND
12	n.c.
13	GND
14	n.c.

Table 10: 14-pin JTAG connector J9.

USB Port

USB data lines of header connector J12[TE0304] are connected (through board-to-board connectors J4[TE0300] and J5[TE0300]) to the USB micro-controller on the TE0300 micromodule.

Pin	Dir.	Signal
1	power I	Vcc
2	I/O	Data-
3	I/O	Data+
4	-	GND
5	-	BRAID

Table 11: connector J12 pin-out.

Header connector J12[TE0304] is a 5-pin 2.54 mm (100 mil) pitch connector compatible with the following industrial USB connectors:

- Bulgin Mini USB Buccaneer PX0443 (IP68 B type Mini USB, front panel mounted, 5 way crimp connector at rear)

Figure 6: Bulgin PX0443 (front connector).

Figure 7: Bulgin PX0443 (rear connector).

- Bulgin Mini USB Buccaneer PX0446 (IP68 B type Mini USB, rear panel mounted, 5 way header connector at rear)

Figure 8: Bulgin PX0446 (front connector).

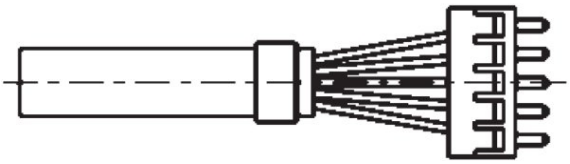


Figure 9: Bulgin PX0446 (rear connector).

If connector J12[TE0304] **is** populated with a 5-pin Bulgin adapter connector, it appears as shown in Figure 10.

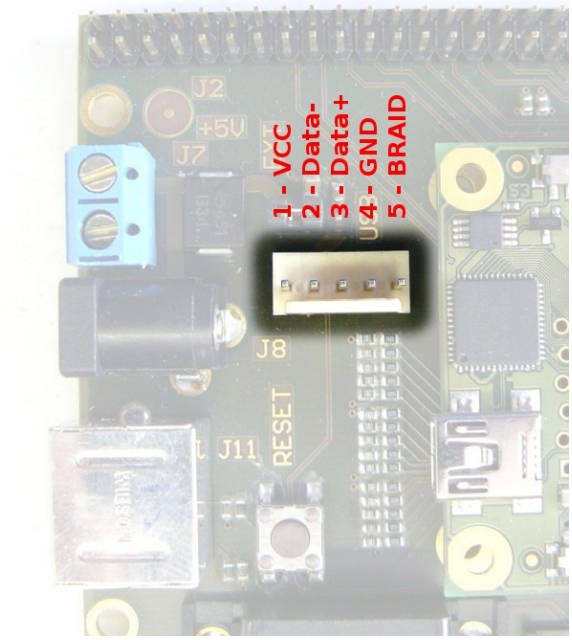


Figure 10: connector J12 [TE0304] when populated.

If connector J12[TE0304] **is not** populated (default assembly), it can be connected to a host USB socket through the J12-to-USB adapter cable (Figure 11) delivered with the TE0304 Demo Carrier Board.

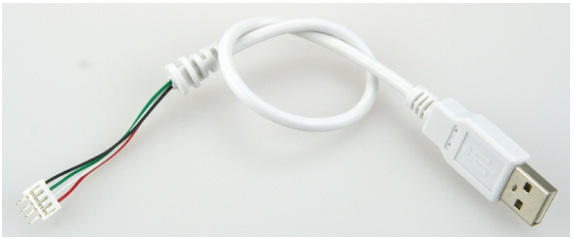


Figure 11: J12-to-USB adapter cable.

When plugging the 4-pin header connector of the adapter cable into the unpopulated connector J12[TE0304], please make sure to

- pull slightly apart the 4 pins in such a way that 4-pin header-pitch matches connector J12 pitch;
- plug the pin corresponding to the red wire in the outermost contact hole (1 - VCC);
- leave the innermost contact (5 - braid) unconnected.

When the adapter cable is inserted into the unpopulated connector J12[TE0304], it should look like shown in Figure 12. The mechanical strain between the two connectors make soldering them unnecessary for most applications.

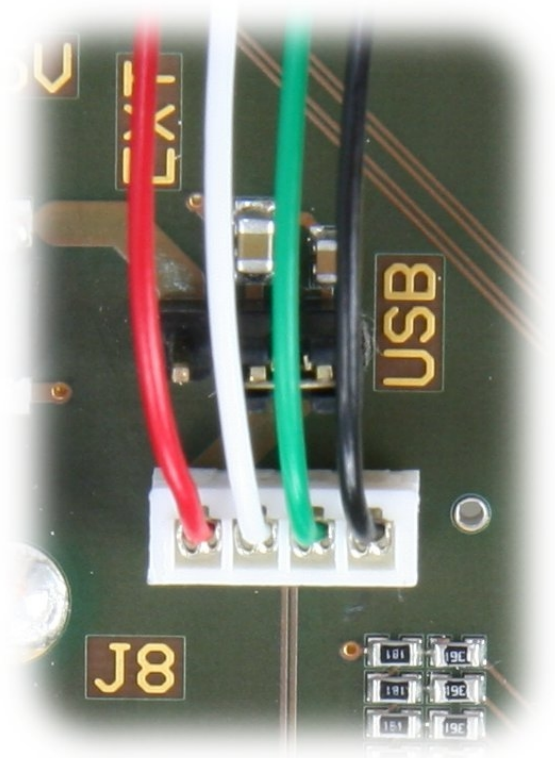


Figure 12: adapter connector in place (board side).

For the USB power line, please see paragraph *USB bus power supply*.

Pushbutton

The pushbutton S1 [TE0304] is connected to the master reset line of the module. By pressing the button, both the EZ-USB FX2 USB microcontroller and the FPGA are reset. The value of the master reset is overridden by switch S2 [TE0300] on the TE0300 micromodule when it is set to *Reset*.

Reference Designs

Genode Labs included some TE0304 reference designs for a range of TE0300 modules to Genode FX project official source tree, and with the next release of Genode FX, the TE0300 support will become a regular part of the official Gen-

ode FX distribution. For furhter information, please consult the following references:

- Genode FX FPGA graphics
- Genode FX project page
- Genode FX project tree
- Genode FX reference UCF files

Ordering Information

Demo Carrier Board

The *Demo Carrier Board* is available at Trenz Eectronic Shop with ordering number **TE0304**. For other kind of headers J2[TE0304] and J4[TE0304], or for other header mounting options, please contact Trenz Electronic.

Optomotive Parts

Optomotive (http://optomotive.si/) is a Slovenian mechatronic company.

The *Cameleon Sensor Head* is available at Trenz Eectronic Shop with ordering number **23367**.

Bulgin Parts

Bulgin (Elektron Components Ltd) is a UK-based company designing and manufacturing electromechanical components. For a comprehensive list of distributors, please visit http://bulgin.co.uk/.

Trenz Electronic Shop

To reach Trenz Eectronic Shop, please visit http://shop.trenz-electronic.de/.

Document Change History

Rev	Date	Who	Description
1.00	2009-06-22	FDR	created
1.01	2009-06-24	FDR	dimensions revised
1.02	2009-06-25	FDR	added differential pairs and single-ended lines details
1.03	2009-07-31	FDR	added pin labels on J12 picture; added J12-to-USB adapter cable
1.04	2009-08-19	FDR	improved TE0304–to-TE0300 pin description

Table 12: document change history

Appendix

The following tables reports pin-out information of the multi-pin connectors J2[TE0304], J4[TE0304] and J5[TE0304].

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	VccIO	-	power I	power I	-	VccIO	2
3	3.3 V	-	power O	power O	-	3.3 V	4
5	GND	-	-	-	-	GND	6
7	B0_IO_C3	C3	IO	IO	C4	B0_IO_C4	8
9	B0_L24_N	B4	IO	IO	A4	B0_L24_P	10
11	B0_L23_N	D5	IO	IO	C5	B0_L23_P	12
13	B0_L20_P	B6	IO	IO	A6	B0_L20_N	14
15	GCLK_L13_N	B9	I	I	B8	GCLK_L13_P	16
17	B3_L02_N	D2	IO	IO	D1	B3_L02_P	18
19	B3_L01_P	C1	IO	IO	C2	B3_L01_N	20
21	B3_L07_P	G6	IO	IO	G5	B3_L07_N	22
23	GND	-	-	-	-	GND	24
25	B3_L03_N	E1	IO	IO	E2	B3_L03_P	26
27	B0_L19_P	F7	IO	IO	E7	B0_L19_N	28
29	B0_L21_N	E6	IO	IO	D6	B0_L21_P	30
31	B0_L18_N	D7	IO	IO	C7	B0_L18_P	32
33	3.3 V	-	power O	power O	-	3.3 V	34
35	B0_L17_N	F8	IO	IO	E8	B0_L17_P	36
37	B0_IO_A8	A8	IO	IO	A7	B0_IO_A7	38
39	GCLK_L14_N	D9	IO	IO	C9	GCLK_L14_P	40

Table 13: pin-out of header J2 [TE0304].

Pin	B2B name	FPGA pin	Dir	Dir	FPGA pin	B2B name	Pin
1	GCLK_L11_P	D10	IO	IO	E10	GCLK_L11_N	2
3	B0_L09_P	C11	IO	IO	D11	B0_L09_N	4
5	GND	-	-	-	-	GND	6
7	B0_IO_A11	A11	IO	IO	G9	B0_IO_G9	8
9	GCLK_L12_N	A10	IO	IO	B10	GCLK_L12_P	10
11	B0_L15_N	F9	IO	IO	E9	B0_L15_P	12
13	2.5 V	-	power O	power O	-	2.5 V	14
15	B0_IO_A12	A12	IO	IO	B11	B0_IO_B11	16
17	B0_L06_N	E12	IO	IO	F12	B0_L06_P	18
19	B0_IO_E13	E13	IO	IO	D13	B0_IO_D13	20
21	B0_L08_N	F11	IO	IO	E11	B0_L08_P	22
23	GND	-	-	-	-	GND	24
25	B0_L05_N	B13	IO	IO	A13	B0_L05_P	26
27	B0_L01_N	A16	IO	IO	B16	B0_L01_P	28
29	B0_L03_N	C14	IO	IO	D14	B0_L03_P	30
31	B0_L04_N	A14	IO	IO	B14	B0_L04_P	32
33	1.2 V	-	power O	power O	-	1.2 V	34
35	Vcon	-	power IO	power O	-	3.3 V	36
37	Vcon	-	power IO	power O	-	5.0 V	38
39	GND	-	-	-	-	GND	40

Table 14: pin-out of header J4 [TE0304].

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	GND	-	-	I	-	DOUT5	2
3	GND	-	-	I	-	DOUT6	4
5	GND	-	-	I	-	DOUT7	6
7	GND	-	-	I	-	DOUT8	8
9	GND	-	-	I	-	DOUT9	10
11	GND	-	-	I	-	LINE_VALID	12
13	GND	-	-	I	-	FRAME_VALID	14
15	GND	-	-	I	-	DOUT0	16
17	GND	-	-	I/O	-	STLN_OUT	18
19	GND	-	-	O	-	EXPOSURE	20
21	GND	-	-	O	-	SCLK	22
23	GND	-	-	I/O	-	STFRM_OUT	24
25	GND	-	-	I/O	-	SDATA	26
27	GND	-	-	O	-	SYSCLK	28
29	GND	-	-	I	-	PIXCLK	30
31	GND	-	-	I	-	DOUT1	32
33	GND	-	-	I	-	DOUT4	34
35	GND	-	-	I	-	DOUT2	36
37	GND	-	-	I	-	DOUT3	38
39	5.0 V	-	power O	power O	-	3.3 V	40

Table 15: pin-out of header J5 [TE0304].